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Design and Construction of a Digital Voltage Duration Counter

Tangsi Rimamsikwe Karma

Nigeria

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***Corresponding author:** Tangsi Rimamsikwe Karma

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Abstract **Original Research Article**

Timing a process is a critical aspect of modern engineering and daily life. Power — a fundamental resource in both developed and developing nations — demands precise duration measurement for industrial, domestic, and billing purposes. This is especially relevant in regions experiencing power supply instability. This paper presents the design and construction of a digital voltage duration counter that records, displays, and stores the duration of a connected A.C. load. The system incorporates a voltmeter for simultaneous voltage measurement and employs the PIC16F84 microcontroller — a mid-range, 8-bit RISC device — as its central processing element. A seven-segment LED display unit renders real-time count output, with a dual-display configuration providing redundancy. The device includes three push-button controls: a Wake/Sleep switch, a Reset switch, and a Dual-Change switch. The maximum measurable duration is determined by the number of display units employed; this implementation used five seven-segment displays, yielding a ceiling of 10,000 seconds. Testing confirmed that the circuit met all design objectives accurately and reliably.

Keywords: voltage duration counter, PIC16F84, microcontroller, seven-segment display, power measurement, EEPROM, assembly language, digital timer.

Introduction

The reliability of electrical power supply is a fundamental prerequisite for economic development, industrial productivity, and household welfare. In many developing nations, however, the power grid is characterised by frequent outages, voltage fluctuations, and unpredictable supply schedules. Nigeria is a particularly well-documented case: the country has for decades struggled with a chronic electricity deficit arising from inadequate generation capacity, ageing transmission infrastructure, and systemic distribution losses (Adenikinju, 2003). These challenges translate directly into measurable economic costs — businesses investing in diesel backup generation, households purchasing battery-powered alternatives, and utility companies losing revenue to unmetered consumption (World Bank, 2009).

Against this backdrop, the need for low-cost, reliable instruments that can accurately record the duration of power availability is both practical and urgent. A voltage duration counter addresses this need by automatically timing the interval during which an A.C. supply is present at a monitored point. Unlike conventional clock-based timers, which run continuously regardless of power status, a voltage duration counter is triggered exclusively by the presence of an A.C. load. This design characteristic makes the device inherently accurate for power-monitoring

purposes: it measures precisely what the end-user needs to know — how long electricity was actually available — without requiring manual start-stop operations (Albert, 2002).

The transition from analog to digital instrumentation has brought significant improvements in timing precision, data storage capability, and resistance to environmental interference. Earlier analog voltage duration meters relied on mechanically driven displays and spring-return mechanisms; their accuracy deteriorated with mechanical wear, and they offered no means of storing historical data. Digital implementations, by contrast, can store accumulated counts in non-volatile memory, display results in unambiguous numerical form, and interface with wider data-acquisition systems if required (Mazidi & Mazidi, 2000). The use of a microcontroller as the central processing element further enhances design flexibility: a single integrated circuit can replace the multiple discrete logic chips that characterised earlier digital timer designs, reducing component count, board area, and potential failure points (Bates, 2004).

This paper presents the complete design and physical construction of a microcontroller-based digital voltage duration counter built around the PIC16F84. The device employs a CD4013 dual D-type flip-flop for A.C. load detection, CD4510 BCD counters for count accumulation, a CD4511 BCD-to-seven-segment decoder/driver, and a five-digit seven-segment LED display array. A regulated 5 V D.C. power supply derived from the mains provides operating power, while a 9 V alkaline battery maintains the stored count in EEPROM during supply interruptions. Three user-operable push-button switches provide Wake/Sleep, Reset, and Dual-Display-Change functions. The design aims to be replicable from locally available components at minimal cost, making it suitable for deployment in resource-constrained environments typical of developing-nation contexts.

The remainder of this paper is organized as follows: the Literature Review section surveys the principal categories of timing technology and their relevance to the present work. The Methodology section details the design of each hardware subsystem and the firmware architecture. The Testing, Results, and Discussion section presents the outcomes of a structured validation programme. The Summary, Conclusion, and Recommendations section synthesizes the findings and proposes directions for future development.

Literature Review

Overview of Timer Technologies

The concept of measuring elapsed time has driven technological innovation from the earliest water clocks of antiquity through the atomic frequency standards of the present day. In the context of electronic engineering, a timer is most broadly defined as a device that measures or controls the duration of a process, generates time delays, or counts events occurring within a defined interval (Taub & Schilling, 1977). Electronic timers now pervade virtually every domain of human activity: they regulate the brewing cycle of a coffee machine, coordinate the switching of high-voltage power-system relays, and maintain the precise microsecond timing required by digital communication networks. The taxonomy of timer technologies can be organized into four principal categories — mechanical, electromechanical, electronic, and computer-based — each representing a distinct stage in the progressive substitution of physical mechanisms by electronic processes (Wikipedia, 2012).

Mechanical Timers

Mechanical timers derive their timing action from the controlled release of stored mechanical energy. The simplest variants use a wound spring that uncoils at a rate governed by an escapement mechanism; when the spring is fully released, a trip lever activates a switch or indicator. Clock-face timers extend this principle by coupling the escapement to a display dial calibrated in seconds or minutes. Dashpot timers introduce a fluidic or pneumatic retarding element: compressed air or hydraulic fluid passes through an adjustable orifice, and the rate of flow determines the timing interval. These devices require no electrical supply and can therefore function in environments where power is unavailable or where electrical ignition hazards

exist, such as in explosive atmospheres (Boylestad & Nashelsky, 2009). Their principal limitations are finite mechanical precision, susceptibility to wear, sensitivity to temperature-induced changes in spring stiffness or fluid viscosity, and the inability to interface with digital data systems without additional transducer circuitry.

Electromechanical Timers

Electromechanical timers emerged in the early twentieth century as designers sought to combine the reliability of mechanical energy storage with the controllability of electrical signals. Synchronous motor timers exploit the fixed relationship between mains frequency and motor shaft speed: the synchronous motor rotates at exactly 50 or 60 revolutions per second (depending on the supply frequency), and a gear train reduces this to the desired timing range with high accuracy as long as the mains frequency is stable. Motor-driven cam timers operate on the same principle, using eccentric cams to operate a sequence of microswitches at programmable points in the rotation cycle (Jones, 1986). The widespread adoption of electromechanical timers in industrial process control during the mid-twentieth century was driven by their robustness under vibration, their ability to switch high currents directly, and the availability of standardised relay socket formats that simplified field replacement. The main disadvantages — mechanical wear of contacts, audible noise, and relatively slow response times measured in milliseconds — became increasingly problematic as electronics moved toward higher switching speeds and quieter operation, ultimately motivating the transition to solid-state designs (Petruzella, 2005).

Electronic Timers

The introduction of semiconductor devices enabled a new generation of timers with no moving parts, negligible wear, and timing resolutions extending from nanoseconds to hours within a single integrated circuit. The fundamental building block of most discrete electronic timers is the RC (resistor-capacitor) network: a capacitor charges or discharges through a resistor at an exponential rate characterised by the time constant $\tau = RC$, and a comparator or threshold detector signals the completion of the timing interval when the capacitor voltage crosses a reference level (Horowitz & Hill, 2015). The NE555 timer IC, introduced by Signetics in 1972, packaged this principle with a comparator, flip-flop, output driver, and discharge transistor into a single 8-pin DIP device. Its availability, low cost, and versatility — supporting monostable, astable, and bistable operating modes — made it the dominant timing element in discrete electronics for several decades (Sehrz, 2002; Green, 1998). In the astable mode, the 555 generates a continuous rectangular waveform whose frequency is determined by the values of two external resistors and a capacitor; in the monostable mode, it generates a single output pulse of precisely controlled duration following a trigger event. These properties made it well suited to simple voltage duration timing when combined with appropriate detection and counting circuitry.

Digital counting timers represent a further evolutionary step. Rather than converting time into an analog voltage level, they count oscillator pulses at a known frequency and display the accumulated count directly. A precision oscillator — typically a quartz crystal or ceramic resonator — provides the timing reference; binary or BCD counters accumulate the pulse count; and a decoder/driver converts the count into a human-readable display. This approach eliminates the non-linearity and temperature sensitivity inherent in RC-based designs and achieves timing accuracies of better than ±50 ppm with a standard quartz crystal (Floyd, 2012). The digital architecture also facilitates the addition of non-volatile memory, serial communication, and programmable alarm thresholds — features that are difficult or impossible to implement in purely analog timer circuits.

Voltage Duration Timers

A voltage duration timer is a specialized sub-class of electronic timer whose primary function is to accumulate and display the total time for which a monitored A.C. voltage has been

present. The timer starts automatically when the supply voltage rises above a detection threshold and halts when the voltage falls below that threshold. The accumulated duration is preserved in non-volatile memory so that it survives supply interruptions and can be reviewed at any subsequent time. Applications include utility billing verification, industrial process-time auditing, generator run-time logging, and consumer advocacy in regions where power companies underreport outage durations (Albert, 2002). The International Energy Agency has identified inadequate metering infrastructure as a major impediment to rational energy-sector reform in sub-Saharan Africa, arguing that without reliable consumption and availability data, neither demand-side management nor performance-based regulation of utilities can be implemented effectively (International Energy Agency, 2019). A low-cost voltage duration counter of the type described in this paper represents a partial solution to this metering gap, providing verifiable availability data at a fraction of the cost of a full smart meter.

Computer-Based Timers and Microcontroller Implementations

Modern embedded systems incorporate programmable timer peripherals as standard features of their microcontroller architectures. A typical hardware timer consists of a multi-bit register that is clocked by the processor oscillator (often through a programmable prescaler) and that generates an interrupt upon overflow or upon match with a compare register. By selecting the prescaler value and compare threshold, the programmer can set the timer period to any value that is an integer multiple of the oscillator period (Microchip Technology, 2001). This programmability makes hardware timers far more flexible than fixed-frequency discrete oscillators, and it allows a single microcontroller to simultaneously manage multiple independent timing tasks by assigning different compare registers to different purposes.

The PIC16F84, selected for the present project, was introduced by Microchip Technology in the 1990s and rapidly became one of the most widely used microcontrollers in educational and small-scale professional applications. Its RISC instruction set of only 35 instructions minimizes the learning curve while the Harvard architecture — separate program and data buses — allows instruction fetch and execution to overlap, providing single-cycle throughput for most instructions (Barnett et al., 2004). The availability of comprehensive application notes, a mature assembler toolchain, and low-cost in-circuit programming adapters further reduced the barriers to adoption. Several prior studies have demonstrated the suitability of the PIC family for low-cost instrumentation tasks in developing-country contexts, including solar charge controllers (Ogunjuyigbe et al., 2016), automatic voltage stabilizers, and data-logging systems for agricultural and environmental monitoring. The present work extends this body of practice to the specific application of power-availability metering.

Methodology

System Architecture

The voltage duration counter was designed as a modular system comprising five discrete functional blocks, each individually characterised before system integration. The five blocks are: (i) a regulated D.C. power supply; (ii) an A.C. load detector based on the CD4013 dual D-type flip-flop; (iii) the PIC16F84 microcontroller, which implements the timing and memory-management firmware; (iv) cascaded CD4510 BCD counters driven by the CD4511 BCD-to-seven-segment decoder; and (v) a five-digit common-cathode seven-segment LED display array. A 9 V alkaline battery, connected in parallel with the EEPROM supply rail through a blocking diode, provides backup power sufficient to retain the stored count for the service life of the battery (approximately 12 months under standby conditions). Table 3 provides a consolidated listing of all principal components with their specifications and functional roles.

Table 3. Principal Hardware Components and Their Functions

Component	Model / Specification	Function
Microcontroller	PIC16F84	Central processing unit
Flip-flop	CD4013	Input detection
BCD Counter	CD4510	Counting & display drive
Display Driver	CD4511	BCD-to-7-segment decode
Display	7-segment LED (×5)	Visual numeric output
Voltage Regulator	LM7805	5 V D.C. regulation
Transformer	220/240 V → 12 V, 300 mA	Mains step-down
Backup Battery	9 V alkaline	EEPROM retention backup

Power Supply Design

The power supply stage is responsible for converting the 220–240 V, 50 Hz A.C. mains supply to a stable, well-regulated 5 V D.C. output capable of sustaining the full system current demand under worst-case conditions. The design follows a conventional linear regulator topology: step-down transformer → full-wave bridge rectifier → bulk smoothing capacitor → three-terminal linear regulator. This topology was chosen in preference to a switching mode power supply (SMPS) because the circuit generates less high-frequency electromagnetic interference — an important consideration given the sensitivity of the CMOS logic devices and the ceramic resonator oscillator circuit to noise coupling (Dorf & Svoboda, 2010).

The mains transformer has a primary rated for 220/240 V and a secondary rated at 12 V, 300 mA. The voltampere rating of the secondary winding and the primary current were determined from the target load power and the assumed transformer efficiency of $\eta = 0.8$, as expressed in Equations 1 and 2:

$$Wp = VA / \eta = (12 \times 0.3) / 0.8 = 4.5\ VA \quad \text{(Eq. 1)}$$

$$I_1 = V_2 I_2 / V_1 = (12 \times 0.3) / 220 \approx 16\ mA \quad \text{(Eq. 2)}$$

The four-diode bridge rectifier produces a pulsating D.C. output with a peak voltage of approximately $12 \times \sqrt{2} - 1.4 = 15.6$ V (allowing for the combined forward voltage drop of two conducting diodes). A 2,200 µF / 25 V electrolytic capacitor smooths this pulsating waveform; the resulting peak-to-peak ripple voltage Vr at full load is given by Equation 3:

$$Vr = I\_load / (f \times C) = 0.3 / (50 \times 2200 \times 10^{-6}) \approx 2.7\ V \quad \text{(Eq. 3)}$$

The ripple voltage of 2.7 V leaves the capacitor voltage in the range 12.9–15.6 V, well above the minimum input voltage required by the LM7805 (7 V) even at the worst-case mains voltage of 200 V. The LM7805 regulates the output to 5.0 V ± 4% and provides thermal shutdown and current-limiting protection. A 100 nF ceramic decoupling capacitor placed directly at the LM7805 output pin suppresses high-frequency noise on the regulated rail. The protection diode (1N4007, reverse-voltage rated at 1,000 V) placed across the regulator input prevents damage should the 9 V backup battery be connected in reverse polarity.

Microcontroller: PIC16F84

The PIC16F84 is the central intelligence of the system. Its 8-bit RISC core executes the 35-instruction set with a four-stage pipeline, achieving an effective instruction throughput of one instruction per machine cycle (4 oscillator periods). At the selected oscillator frequency of 4 MHz, the machine cycle period is 1 µs, and most instructions complete in a single machine

cycle (two cycles for branch instructions). Table 4 lists the key internal registers used by the firmware, together with their addresses in the PIC16F84's special function register (SFR) space.

Table 4. Key PIC16F84 Special Function Registers Used in Firmware

Register	Address	Description
TMR0	0x01	8-bit free-run timer / counter
INTCON	0x0B	Interrupt control: GIE, TOIE, TOIF flags
EEDATA	0x08	EEPROM data register
EEADR	0x09	EEPROM address register
EECON1	0x88	EEPROM control: RD, WR, WREN, EEIF flags
PORTA	0x05	5-bit bidirectional port (RA0–RA4)
PORTB	0x06	8-bit bidirectional port (RB0–RB7)
STATUS	0x03	ALU status: C, DC, Z, RP0, RP1 bits

The EEPROM of the PIC16F84 comprises 64 bytes of byte-erasable, byte-programmable non-volatile storage with a guaranteed data retention of 40 years and an endurance of at least 10^6 write cycles per byte (Microchip Technology, 2001). These specifications are more than adequate for the present application, in which the stored count is updated at most once per second during normal operation and once per power interruption event. The watchdog timer (WDT) is enabled in the configuration word programmed alongside the application firmware; if the firmware fails to clear the WDT within the selected 18 ms timeout window, the microcontroller is automatically reset to a known good state — an important safety feature for an instrument that may operate unattended for extended periods.

Input Detection: IC CD4013 Dual D Flip-Flop

Reliable detection of the presence or absence of the monitored A.C. supply is critical to the accuracy of the voltage duration measurement. A direct connection between the mains A.C. signal and the microcontroller's digital input pins is not feasible because the mains voltage (220–240 V) far exceeds the PIC16F84's maximum input voltage of 5.5 V. The detection circuit therefore uses a potential-divider and rectifier network to derive a 0–5 V D.C. signal that represents the presence of the A.C. supply, and this signal drives the clock input of one half of the CD4013 dual D-type flip-flop (Fairchild Semiconductor, 2000).

The D-type flip-flop changes state on the rising edge of its clock input. When the monitored A.C. supply is present, the rectified and divided signal alternates between logic 0 and logic 1 at 50 Hz, causing the flip-flop to toggle on every positive transition. The Q output of the flip-flop is connected to a microcontroller interrupt pin and serves as the primary start signal for the timing firmware. When the A.C. supply is removed, the clock input remains at logic 0, the flip-flop holds its last state, and the microcontroller detects the static condition as an absence of supply, triggering the hold sequence. The second flip-flop in the CD4013 provides a complementary

latch function for the Wake/Sleep control line, ensuring that the user-operated switch does not corrupt the accumulated count stored in EEPROM.

BCD Counter: CD4510

The CD4510 presettable BCD up/down counter serves as the interface between the microcontroller's output port and the seven-segment display driver. In the present design, the PIC16F84 outputs a 4-bit BCD value on four PORT B lines; the CD4510 latches this value on the rising edge of a load-enable strobe. Five CD4510 devices are cascaded in sequence by connecting the carry-out of each stage to the clock input of the next, forming a five-decade counter chain capable of representing values from 00000 to 99999 seconds. Only the lower 10,000-second range (0–9,999) is used in practice, corresponding to the design ceiling of the five-display array. The up/down control pin is permanently tied to logic 1 (up-count mode), and the reset pin is driven by the firmware Reset routine when the user activates the Reset push-button (Floyd, 2012).

Each CD4510's BCD output is connected to the input of a CD4511 BCD-to-seven-segment latch/decoder/driver. The CD4511 converts the 4-bit BCD input into the seven segment-drive signals (a through g) required by the common-cathode LED display. The latch input of the CD4511 is tied permanently to logic 1, so the segment outputs track the BCD inputs without latching delay. The lamp-test (LT) and blanking (BL) inputs are tied to logic 1 to enable normal display operation. The CD4511 can sink up to 25 mA per segment output, which is comfortably within the rating of the LED segments and the series current-limiting resistors (Tokheim, 1999).

Display: Seven-Segment LED Array

The five seven-segment display units selected for this design are common-cathode devices with a forward segment voltage of 2.0 V (typical) and a maximum continuous segment current of 10 mA. The common cathode of each display is connected directly to circuit ground; all cathodes are therefore permanently active, and the display multiplexing (if required) is handled by selectively enabling segment drivers rather than by cathode switching. For this single-digit-always-on configuration, the segment current for each active segment is limited by a series resistor calculated from Equation 4:

$$R_{seg} = (V_{supply} - V_F) / I_F = (5 - 2.0) / 0.010 = 300\ \Omega \rightarrow 470\ \Omega \text{ (standard value)} \quad \text{(Eq. 4)}$$

A 470 Ω resistor is used in practice, reducing the segment current to approximately 6.4 mA — within the device rating and producing adequate luminance for indoor reading in ambient lighting conditions. The five displays are physically arranged in a horizontal row within the transparent display window cut into the enclosure front panel. The leftmost digit represents the ten-thousands place, and the rightmost digit represents the units (seconds) place. A decimal point LED embedded in the central display unit is used as a status indicator: steady illumination indicates normal counting mode, while flashing at 1 Hz indicates that the Wake/Sleep standby mode is active (Kingbright Corporation, 1999).

Software Design and Firmware Architecture

The firmware was developed in PIC assembly language using the MPASM assembler distributed with Microchip's MPLAB IDE (version 5.70). Assembly language was selected in preference to a high-level language (e.g., C) because the limited RAM of the PIC16F84 (68 bytes) and the need for cycle-accurate timing in the ISR make manual register management essential; a C compiler for this device would consume a significant fraction of available RAM for the runtime stack and calling convention overhead (Hintz & Tabak, 1992). The firmware is structured into four layers: initialisation, main loop, interrupt service routine, and utility subroutines.

Initialisation configures all I/O pin directions via the TRISA and TRISB registers, sets the TMR0 prescaler to divide-by-256 (yielding a timer overflow every 65.536 ms at 4 MHz), enables global and timer overflow interrupts in INTCON, reads the last stored count from EEPROM into RAM working registers, and

transfers the recovered count to the display output ports before entering the main loop.

The main loop continuously polls the state of the flip-flop output (A.C. supply present or absent) and the three push-button inputs. When the A.C. supply is detected as present, the COUNTING flag is set and the ISR is permitted to increment the count. When the supply is detected as absent, the COUNTING flag is cleared, the current count is written to EEPROM via the EECON1/EECON2 handshake, and the main loop enters the hold state. The Reset button clears the COUNTER register, writes zero to EEPROM, and resets all five display digits. The Dual-Change button toggles the active display between the primary and secondary seven-segment arrays, providing the built-in redundancy function.

The ISR fires every 65.536 ms (approximately 15.3 times per second) on TMR0 overflow. A software counter (TICK_COUNT) in RAM is decremented on each ISR entry; when TICK_COUNT reaches zero, it is reloaded with the value 15 (representing 15 ISR periods ≈ 0.983 s, adjusted to 16 periods every 16th second to compensate for the non-integer ratio), and the one-second increment routine is called. This approach avoids the need for an external real-time clock chip while maintaining sub-1% timing accuracy compatible with the ceramic resonator tolerance. The ISR also refreshes the display by writing the decimal-decomposed digits of the current count to the PORT B output lines and issuing a CD4510 load-enable strobe.

Casing and Physical Construction

The completed PCB and all passive components were housed in an ABS plastic enclosure with external dimensions of 23 cm × 23 cm × 15 cm. ABS was selected for its combination of mechanical rigidity, electrical insulating properties, and ease of cutting with standard workshop tools. The enclosure wall thickness of 3 mm provides adequate mechanical protection against incidental impacts during field installation. All mains-voltage wiring within the enclosure was dressed away from the low-voltage PCB and secured with insulated cable ties to prevent accidental contact with the display wiring harness. Creepage and clearance distances between mains-voltage conductors and the low-voltage circuit were maintained at a minimum of 8 mm in accordance with basic insulation requirements for SELV (Safety Extra-Low Voltage) circuits (Dorf & Svoboda, 2010).

Three rectangular apertures of 12 mm × 12 mm were cut in the front panel for the push-button switches, which were mounted on a sub-panel of 1.5 mm aluminium sheet bonded to the inner face of the enclosure. A single rectangular aperture of 100 mm × 20 mm was cut for the display window, over which a 3 mm clear acrylic sheet was bonded with solvent cement to provide mechanical protection and act as a diffuser for the LED segments. The PCB was secured to the base of the enclosure on four M3 × 10 mm nylon standoffs, providing a 10 mm air gap between the PCB and the enclosure base for ventilation and to prevent electrostatic discharge coupling.

Testing, Results, and Discussion

Testing Procedure

The system was validated through a structured four-stage test programme designed to detect faults at each level of the design hierarchy before progressing to the next level of integration. Stage 1 consisted of firmware verification: the assembly source was assembled using MPASM and the resulting .HEX file was loaded into the MPLAB simulator for instruction-level trace debugging. Boundary conditions — including TMR0 overflow, EEPROM write, and push-button debounce — were verified in simulation before any hardware was assembled. Stage 2 was behavioural simulation of the complete circuit using Electronic Workbench 8, which allowed the interaction between the PIC16F84 model, the CD4013, CD4510, and CD4511 models, and the simulated LED display to be observed under controlled stimulus conditions. Stage 3 was breadboard prototyping: the circuit was assembled on a solderless breadboard and operated from a bench power supply, allowing individual signals to be probed with a logic analyser and oscilloscope. Stage 4 comprised formal measurements on the final soldered PCB, including insulation resistance testing (100 V D.C., minimum 1 MΩ between mains conductors

and the low-voltage rail), port voltage measurements, and duration accuracy trials.

Microcontroller Port Voltages

The output voltages at each microcontroller port were measured under two conditions: (a) output pin driving logic HIGH (source mode), and (b) output pin driving logic LOW (sink mode). A calibrated Fluke 87V True-RMS multimeter was used for all voltage measurements. Table 1 reports the recorded values against the PIC16F84 datasheet specification of 2.0–5.0 V for logic HIGH outputs at a 5 V supply. All ports fell within the specified range, confirming adequate output drive strength for the downstream CMOS logic devices.

Table 1. Sink and Source Voltages at Microcontroller Ports

Port	Reference Output (V)	Recorded Value (V)
A	2 – 5	2.5 – 5
B	2 – 5	2.5 – 5
C	2 – 5	2.5 – 5

Seven-Segment Display Logic Verification

The segment-drive logic of the CD4511 was verified by applying each of the ten BCD input codes (0000_2 through 1001_2) in sequence and recording the resulting illuminated segments against the expected seven-segment code for each decimal digit. A logic probe was used to confirm the state of each segment output, and the physical display was inspected visually for correct digit formation. Table 2 summarises the logic-level verification for the HIGH and LOW conditions; no discrepancies were found between expected and recorded values for any of the ten digit codes tested.

Table 2. Seven-Segment Display Logic States

Impulse	Standard	Recorded	Interpretation
HIGH	1	1	ON (LED illuminated)
LOW	0	0	OFF (LED dark)

Duration Accuracy Test

Timing accuracy was assessed by operating the counter for a reference interval of exactly 3,600 seconds (one hour), measured concurrently by a calibrated GPS-disciplined frequency counter with a traceable accuracy of $\pm 1 \times 10^{-9}$. The device was started and stopped synchronously with the reference counter using the A.C. supply as the common trigger, ensuring that the measurement window was identical for both instruments. The test was repeated across ten independent trials under ambient laboratory conditions (temperature 22°C ± 2°C, relative humidity 55% ± 10%). Table 5 records the device reading, error, and percentage error for each trial.

Table 5. Duration Accuracy Test Results Over Ten Trials

Trial	Reference (s)	Device Reading (s)	Error (s)	Error (%)
1	3600	3599	1	0.028
2	3600	3599	1	0.028
3	3600	3599	1	0.028
4	3600	3599	1	0.028
5	3600	3599	1	0.028
6	3600	3599	1	0.028
7	3600	3599	1	0.028
8	3600	3599	1	0.028
9	3600	3599	1	0.028
10	3600	3599	1	0.028
Mean	3600	3599	1.0	0.028

The device consistently recorded 3,599 seconds against the 3,600-second reference, yielding a systematic under-count of one second per hour (0.028%). This systematic error is attributable to the compensation algorithm in the ISR: the software accumulates 15 tick events per nominal second but does not apply the correction factor until the 16th second in each 16-second cycle, introducing a small but deterministic lag. The error is well within the ±0.5% tolerance of the 4 MHz ceramic resonator and is negligible for the target application. Over a 24-hour measurement period, the cumulative error would amount to 24 seconds — less than 0.03% of the total duration. Replacement of the ceramic resonator with a ±50 ppm quartz crystal would reduce this systematic error to less than 0.2 seconds per hour.

Load Range Detection Test

The operational load range of the input detection circuit was verified by connecting resistive loads of known power ratings (40 W, 100 W, 500 W, 1,000 W, and 2,000 W) in turn to the monitored supply terminal and confirming that the flip-flop triggered correctly and that the timer started. Table 6 records the supply current corresponding to each load at 220 V and the detection outcome. The circuit detected the A.C. supply presence correctly for all load levels tested, confirming that the detection threshold is set below 40 W — the lowest load level expected in domestic applications (a standard incandescent night-light or LED lamp).

Table 6. Input Detection Performance Across Load Range

Load Power (W)	Supply Current (mA)	Flip-flop Triggered?	Timer Started?
40	182	Yes	Yes
100	455	Yes	Yes
500	2273	Yes	Yes

1000	4545	Yes	Yes
2000	9091	Yes	Yes

EEPROM Retention and Wake/Sleep Function

Non-volatile count retention was evaluated by subjecting the device to 50 deliberate power interruptions applied at randomised intervals during active counting. Following each interruption and subsequent power restoration, the display value was compared with the value recorded by an independent counter running in parallel on a separate system. In all 50 trials, the recovered count matched the reference count exactly, confirming 100% EEPROM write reliability under the test conditions. The minimum write time between interruption and successful EEPROM commit was measured at 10.4 ms, confirming that the firmware completes the EEPROM write cycle before the power supply voltage decays below the PIC16F84's minimum operating voltage of 2 V (supported by the bulk capacitance of the 2,200 µF supply capacitor, which maintains the rail above 2 V for approximately 45 ms after mains removal at full load).

The Wake/Sleep function was tested by activating the Wake/Sleep switch during active counting and verifying that: (a) the display extinguished within one display refresh cycle (< 17 ms); (b) the firmware continued to accumulate elapsed time in the RAM COUNTER register; and (c) reactivating the switch caused the display to resume showing the correct accumulated count. All three conditions were confirmed across 20 consecutive switch activations without error. The reduction in supply current during Sleep mode was measured at 68 mA (display off) compared with 94 mA (display on), representing a 28% reduction in current draw — directly translating into an extended backup battery life of approximately 132 mA·h / 68 mA ≈ 1.9 hours versus 132 mA·h / 94 mA ≈ 1.4 hours for a standard 9 V alkaline battery.

Discussion

The test results collectively confirm that the digital voltage duration counter meets all stated design objectives. Port output voltages were within specification at all test points; the seven-segment display produced correct digit representations for all BCD input codes; and timing accuracy was 99.97% over a one-hour reference interval. The input detection circuit operated reliably across the full range of representative domestic and light-industrial load powers (40 W to 2,000 W), and EEPROM retention was 100% reliable under the 50-trial interruption stress test.

The principal performance limitation of the current design is the systematic one-second-per-hour under-count introduced by the ISR compensation algorithm. This arises because the ratio of the TMR0 overflow interval (65.536 ms) to the desired one-second timing epoch is not a whole number ($65.536 \times 15 = 983$ ms $\neq 1{,}000$ ms), requiring a software correction that is applied discontinuously. A more precise approach would use a 32,768 Hz watch crystal and configure the Timer1 module (available on the PIC16F876 and later devices) in its dedicated low-frequency oscillator mode, which counts 32,768 oscillator pulses per second exactly and therefore requires no software compensation (Microchip Technology, 2001). Implementing this change would reduce the timing error to the crystal's intrinsic frequency tolerance of ±20 ppm — approximately 1.7 ms per day.

A second limitation is the architecture-specific nature of the PIC assembly firmware. The instruction set, register model, and peripheral configuration registers of the PIC16F84 are not compatible with other popular microcontroller families such as the AVR or ARM Cortex-M series. Porting the firmware to a different platform would require a complete rewrite, as there is no binary-compatible upgrade path. For

future versions of the design, implementing the firmware in ANSI C and targeting a microcontroller with a well-supported C compiler (such as the PIC16F18xxx series with XC8) would significantly reduce the porting effort and allow the same firmware to be compiled for multiple target devices with only minor board-specific configuration changes (Bates, 2004).

The cost analysis of the completed prototype, based on retail component prices sourced from local electronics markets in Maiduguri, yielded a total bill of materials cost of approximately ₦4,200 (Nigerian naira) or approximately USD 10 at 2012 exchange rates. This represents a substantial cost reduction compared with imported utility metering equipment, which typically costs USD 50–200 per installation point (World Bank, 2009). The design is therefore economically accessible for small-scale deployment by individual consumers, community cooperatives, or small businesses seeking to document power availability for billing dispute resolution or insurance claims.

Summary, Conclusion, and Recommendations

Summary

This paper has described the complete design, construction, and experimental validation of a microcontroller-based digital voltage duration counter. The system uses the PIC16F84 microcontroller as its central computational element, supported by a CD4013 dual D-type flip-flop for A.C. supply detection, cascaded CD4510 BCD counters for count accumulation, a CD4511 BCD-to-seven-segment decoder/driver, and a five-digit common-cathode seven-segment LED display array. A mains-derived, LM7805-regulated 5 V D.C. supply provides operating power, and a 9 V alkaline backup battery maintains the stored count in EEPROM during supply interruptions. Three user-operable push-button switches provide Wake/Sleep, Reset, and Dual-Display-Change functions. The firmware, written in PIC assembly language, implements a TMR0-overflow-driven timing loop, EEPROM write-back on every supply interruption, and a display refresh routine operating at greater than 60 Hz. The complete prototype was assembled from locally sourced components at a total materials cost of approximately USD 10.

Conclusion

Experimental testing confirmed that the device met all stated design objectives. Timing accuracy was 99.972% over a one-hour reference interval (0.028% error), which is adequate for the target application of domestic and light-industrial power-availability monitoring. The input detection circuit reliably triggered across the full range of representative load powers (40 W to 2,000 W). EEPROM retention was 100% reliable across 50 deliberate power interruption events. Port output voltages and display logic states were verified as conforming to component specifications. The Wake/Sleep function reduced current draw by 28%, extending battery backup life proportionally.

The work demonstrates that a microcontroller-based voltage duration counter can be designed, constructed, and validated using a modest set of off-the-shelf components at a cost accessible to individual consumers in developing-nation contexts. The design contributes to the broader goal of low-cost instrumentation for energy-sector transparency and consumer empowerment in regions characterised by unreliable power supply. The systematic approach adopted — block-level design, simulation before hardware construction, and structured test programme — provides a replicable framework for comparable instrumentation projects in resource-constrained environments.

Recommendations

Based on the findings of this study, the following directions for future development are proposed:

1. Adopting a more capable microcontroller — such as the PIC16F877A or Microchip ATmega328P — would provide additional timer peripherals (including Timer1 with its dedicated 32,768 Hz low-power oscillator mode), multiple UART/SPI/I²C communication ports, and substantially more RAM and Flash,

enabling higher timing accuracy, data logging to external SD cards, and multi-channel monitoring without hardware-imposed constraints.

2. Replacing the five-digit seven-segment array with a 16×2 LCD or 128×64 OLED module would reduce pin-count requirements, allow the display of alphanumeric information (cumulative duration in hours:minutes:seconds, date, power-on event log, and estimated energy consumption in kWh assuming a rated load power), and substantially improve legibility in variable ambient lighting conditions.
3. Implementing a current-transformer (CT) clamp on the monitored supply conductor would allow the device to measure actual load current in addition to voltage presence, enabling true energy measurement (watt-hours) rather than mere voltage duration — a significant capability enhancement for billing and audit applications without requiring physical interruption of the monitored circuit.
4. Adding a relay output module driven by the microcontroller would allow the timer to control an external load automatically: for example, activating a backup generator, switching to an uninterruptible power supply, or sending an alert signal when the mains duration falls below a programmed daily threshold. This would extend the device from a passive measurement instrument to an active power management controller.
5. Integration of a LoRaWAN or NB-IoT wireless module would enable remote telemetry of duration data to a cloud-hosted data aggregation platform, allowing utility companies, regulators, or consumer advocacy groups to compile statistical power-availability data across many geographically dispersed monitoring points without requiring physical site visits (Adoghe et al., 2013). This capability would be particularly valuable for large-scale regulatory compliance monitoring or for academic studies of grid performance in developing-nation contexts.
6. Before any commercial deployment, the device enclosure and internal wiring should be qualified to the IEC 61010-1 safety standard for electrical measurement, control, and laboratory equipment, and the enclosure should be rated to at least IP54 (dust-protected, splash-proof) per IEC 60529. These certifications would ensure that the instrument can be safely installed in uncontrolled indoor environments such as domestic meter cupboards, commercial switchrooms, and light-industrial panels.

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